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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/847,535	05/01/2001	Barry Bond	MS1-665US	4017

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EXAMINER	
STEVENS, THOMAS H	
ART UNIT	PAPER NUMBER
2121	

SHORTENED STATUTORY PERIOD OF RESPONSE	NOTIFICATION DATE	DELIVERY MODE
3 MONTHS	03/28/2007	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Notice of this Office communication was sent electronically on the above-indicated "Notification Date" and has a shortened statutory period for reply of 3 MONTHS from 03/28/2007.

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lhptoms@leehayes.com

Office Action Summary	Application No.	Applicant(s)	
	09/847,535	BOND ET AL.	
	Examiner	Art Unit	
	Thomas H. Stevens	2121	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 January 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-28,34-42 and 45-50* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-28,34-42 and 45-50* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. 1-28, 34-42 and 45-50.

Section I: Non-Final Rejection

Claim Objection

2. The specification is objected to as failing to provide proper antecedent basis for the claimed subject matter. See 37 CFR 1.75(d)(1) and MPEP § 608.01(o). Correction of the following is required: Claim 47 recites a "call-deliver", this phrase is not set forth in the specification. Applicants should note that it is considered inherent that calls must be delivered, otherwise the device would be inoperative.

Claim Rejections - 35 USC § 101

3. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

4. Claims 1-10, 40,41,47,49 are rejected under 35 U.S.C. 101 because these claims are considered to be software per se, as such they are abstract and thus non-statutory subject matter.

5. Claims 11,12,26-28,38,39 and 46 are rejected under 35 U.S.C. 101 because they're directed to a media or medium of a native kernel configured to receive calls from native program modules. This claimed subject matter lacks a practical application of a judicial exception (law of nature, abstract idea, naturally occurring article/phenomenon) since it fails to produce a useful, concrete and tangible result.

Specifically, the claimed subject matter does not produce a tangible result because the claimed subject matter fails to produce a result that is limited to having real world value rather than a result that may be interpreted to be abstract in nature as, for example, a thought, a computation, or manipulated data. More specifically, the claimed subject matter provides for electronic interaction between native and non-native by way of a medium or medium, by way of a carrier signal.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 13-25, 34-37, 48, 50 rejected under 35 U.S.C. 102(b) as being anticipated by Davidian (US Patent 5,623,617; hereafter Davidian). Davidian teaches an emulator performance instruction sequence (abstract).

Claim 13. A method of emulating (column 3, lines 37-40) a kernel for non-native program modules (in this instance the 68020 processor is the guest instruction, column 4, lines 50-52), the method comprising: intercepting (host or native program receiving instruction pointers from the guest or non-native, column 3, lines 16-3) kernel calls from non-native program modules (in this instance the 68020 processor is the guest

instruction, column 4, lines 50-52), the kernel calls calling a kernel emulator (column 3, lines 37-40) comprising software converting (teaching of caching routing used to retrieve the code between the 32 and 64 byte code blocks, column 5 ,lines 35-53) the intercepted non-native kernel calls (in this instance the 65536 processor is the host instruction, column 4, lines 49-50) into native kernel calls (in this instance the 65536 processor is the host instruction, column 4, lines 49-50).

Claim 14. A method as recited in claim 13, wherein the converting (teaching of caching routing used to retrieve the code between the 32 and 64 byte code blocks, column 5 ,lines 35-53) step comprises translating ("decoding" of the guest instruction, column 6, lines 1-14) a non-native paradigm (in this instance the 65536 processor is the host instruction, column 4, lines 49-50) for passing parameters (e.g., native routines, column 5 ,lines 25-30) into a native paradigm for passing parameters (e.g., native routines, column 5, lines 25-30).

Claim 15. A method as recited in claim 13, wherein the converting (teaching of caching routing used to retrieve the code between the 32 and 64 byte code blocks, column 5 ,lines 35-53) step comprises translating ("decoding" of the guest instruction, column 6, lines 1-14) non-native CPU instructions ("emulation routines", column 5, lines 54-58) into native CPU instructions.

Claim 16. A method as recited in claim the converting step comprises translating ("decoding" of the guest instruction, column 6, lines 1-14) addresses from length into native length ("emulation blocks packed into aligned 32 and 64 byte blocks", bytes=words column 5, lines 46-53).

Claim 17. A method as recited in claim 13, wherein the converting (teaching of caching routing used to retrieve the code between the 32 and 64 byte code blocks, column 5 ,lines 35-53) step comprises translating ("decoding" of the guest instruction, column 6, lines 1-14) words from non-native word size into native word size ("emulation blocks packed into aligned 32 and 64 byte blocks", bytes=words column 5, lines 46-53).

Claim 18. A method as recited in claim 13 further comprising limiting addressable ("host addressable memory", column 2, lines 53-63) memory to a range addressable ("host addressable memory", column 2, lines 53-63) by non-native program modules.

Claim 19. A method as recited in claim 13 further comprising synchronizing a native shared data structure ("emulation blocks packed into aligned 32 and 64 byte blocks", column 5, lines 46-53) with a non-native shared data structure.

Claim 20. A method as recited claim 13 further comprising mapping versions of process shared data structures ("emulation blocks packed into aligned 32 and 64 byte blocks",

column 5, lines 46-53)(SDSs) between native and non-native program modules (in this instance the 68020 processor is the guest instruction, column 4, lines 50-52).

Claim 21. A method as recited in claim 20, wherein a process SDS ("emulation blocks packed into aligned 32 and 64 byte blocks", column 5, lines 46-53) of a native program module includes a pointer (column 6, lines 28-34) to a process SDS ("emulation blocks packed into aligned 32 and 64 byte blocks", column 5, lines 46-53) of a non-native program module.

Claim 22. A method as recited in claim 20, wherein a process SDS ("emulation blocks packed into aligned 32 and 64 byte blocks", column 5, lines 46-53) of a non-native program module includes a pointer (column 6, lines 28-34) to a process SDS ("emulation blocks packed into aligned 32 and 64 byte blocks", column 5, lines 46-53) of a native program module.

Claim 23. A method as recited in claim 13 further comprising mapping versions of thread shared data structures ("emulation blocks packed into aligned 32 and 64 byte blocks", column 5, lines 46-53)(SDSs) data structure between native and non-native program modules (in this instance the 68020 processor is the guest instruction, column 4, lines 50-52).

Claim 24. A method as recited in claim 23, wherein a thread SDS ("emulation blocks packed into aligned 32 and 64 byte blocks", column 5, lines 46-53) of a native program module includes a pointer (column 6, lines 28-34) to a thread SDS ("emulation blocks packed into aligned 32 and 64 byte blocks", column 5, lines 46-53) of a non-native program module.

Claim 25. A method as recited in claim 23, wherein a thread SDS of a non-native program module includes a pointer (column 6, lines 28-34) to a thread SDS ("emulation blocks packed into aligned 32 and 64 byte blocks", column 5, lines 46-53) of a native program module.

Claim 34. A method comprising emulating (column 3, lines 37-40) a non-native kernel for a native computing platform so that kernel calls from non-native applications are translated ("decoding" of the guest instruction, column 6, lines 1-14) words into calls to a native kernel, the native kernel emulator (column 3, lines 37-40) comprising software.

Claim 35. A method as recited in claim 34, wherein the emulating (column 3, lines 37-40) step comprises: translating ("decoding" of the guest instruction, column 6, lines 1-14) non-native CPU instructions ("emulation routines", column 5, lines 54-58) into native CPU instructions ("emulation routines", column 5, lines 54-58)words; translating ("decoding" of the guest instruction, column 6, lines 1-14) addresses from non-native length into native length; limiting addressable ("host addressable memory", column 2,

lines 53-63) memory to a range addressable ("host addressable memory", column 2, lines 53-63) by non-native program modules (in this instance the 68020 processor is the guest instruction, column 4, lines 50-52).

Claim 36. A method as recited in claim 35, wherein the emulating (column 3, lines 37-40) step further comprises translating ("decoding" of the guest instruction, column 6, lines 1-14) a non-native paradigm for passing parameters (e.g., native routines, column 5 ,lines 25-30) into a native paradigm for passing parameters (e.g., native routines, column 5 ,lines 25-30).

Claim 37. A method as recited in claim 34, wherein the converting step further comprises translating ("decoding" of the guest instruction, column 6, lines 1-14) words from non-native word size into native word size.

Claim 48. A method comprising emulating (column 3, lines 37-40) a non-native kernel for a native computing platform so that kernel calls from non-native applications are translated ("decoding" of the guest instruction, column 6, lines 1-14) into calls to a native kernel, the native kernel emulator (column 3, lines 37-40).

Claim 50. A method of emulating (column 3, lines 37-40) a kernel for non-native program modules (in this instance the 68020 processor is the guest instruction, column 4, lines 50-52) thereby enabling applications dependent on non-native kernel calls (in

this instance the 65536 processor is the host instruction, column 4, lines 49-50) to execute independent of the kernel for non-native program modules (in this instance the 68020 processor is the guest instruction, column 4, lines 50-52), the method being implemented at least partially by a computer, the method comprising: intercepting (host or native program receiving instruction pointers from the guest or non-native, column 3, lines 16-31) kernel calls from non-native program kernel calls calling a kernel emulator (column 3, lines 37-40) comprising software; calls; modules, the converting the intercepted non-native kernel calls (in this instance the 65536 processor is the host instruction, column 4, lines 49-50) into native kernel outputting the native kernel calls (in this instance the 65536 processor is the host instruction, column 4, lines 49-50).

Section II: Response to Arguments

Claim Objections

8. Applicants are thanked for responding to these issues; however, the objections to claims 29-33 remain outstanding. The objections as set forth in the previous office action stand. Note: **Per 37 CFR 1.121** states the following: *No claim text shall be presented for any claim in the claim listing with the status of "canceled" or "not entered."*

101

9. Applicants are thanked for responding to this issue; however, the arguments presented are non-persuasive for the reasons as set forth above.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicants' disclosure:

- US Patent 5,751,982 teaches software emulation system with dynamic translation of emulated instructions for increased processing speed.
- US Patent 5,796,989 teaches a method for increasing cache efficiency during emulation through operation code organization.
- US Patent 6,363,409 teaches automatic client/server translation and execution of non-native applications.
- US Patent 5,632,028 teaches a system and method in providing fast software emulation of unimplemented instructions.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mr. Tom Stevens whose telephone number is 571-272-3715, Monday-Friday (7:00 am- 4:30 pm EST).

If attempts to reach the examiner by telephone are unsuccessful, please contact examiner's supervisor Mr. Anthony Knight 571-272-3687. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov.. Answers to questions regarding access to the Private PAIR system, contact the Electronic Business Center (EBC) (toll-free (866-217-9197)).

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Tech Center 2100